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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,525	03/23/2004	Earl Schreyer	24317/81002	3440

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SIDLEY AUSTIN LLP
555 CALIFORNIA STREET
SUITE 2000
SAN FRANCISCO, CA 94104-1715

EXAMINER	
HOLTON, STEVEN E	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/807,525	SCHREYER ET AL.	
	Examiner	Art Unit	
	Steven E. Holton	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *219-245* is/are pending in the application.

4a) Of the above claim(s) *219-233 and 242-245* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *234 and 237-241* is/are rejected.

7)☒ Claim(s) *235 and 236* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Species V in the reply filed on 5/1/2008 is acknowledged.

Information Disclosure Statement

2. The information disclosure statements (IDS) submitted on 3/23/2004 and 6/4/2008 were considered by the Examiner. The IDS filed on 2/23/2004 contained IDS statements and reference cited documents pertaining to the parent application, 09/658707. These references have been considered in regard with the current application. The Examiner notes that the references on the IDS filed on 6/4/2008 are primarily concerned with AC to DC power conversion circuits and not analog to digital conversion circuits and the submitted references are not closely related to the disclosed invention.

Specification

The abstract of the disclosure is objected to because the abstract is greater than 150 words long. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 238-241 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 238 and 240 recites the limitation "digital decoder" in line 1. There is insufficient antecedent basis for this limitation in the claim. Claims 239 and 241 are dependent on claims 238 and 240 and are therefore similarly rejected. The Examiner assumes that the 'digital decoder' is intended to be the 'digital encoder' named in claim 234.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 234 and 247 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hara et al. (USPN: 6686969), hereinafter Hara, in view of van de Plassche (USPN: 4831379), and in further view of Vorenkamp et al. (USPN: 5751236), hereinafter Vorenkamp.

Regarding claim 234, Hara discloses a graphics digitizer comprising a channel with an input of an analog video signal (Fig. 1, the input labeled Video Signal) and an output of a digital video signal (Fig. 1, the output of the A/D converter); a phase locked loop coupled to a horizontal sync signal providing a sampling clock frequency (Fig. 1, element 6 is a PLL with input HD and output to the A/D converter); a timing generator circuit that receives the horizontal sync signal and the sampling clock frequency (Fig. 1, element 4 takes in HD and the sampling signal and outputs driving clock signals for operating the display); and an analog-to-digital converter that receives the analog video signal and outputs a digital video signal (Fig. 1, element 1).

However, Hara does not disclose the specific circuit elements within the analog-to-digital converter.

Van de Plassche discloses an analog-to-digital converter that takes in an analog input signal (Fig. 3, element VI) and comprises a reference generator that receives a reference voltage and generates a set of differential reference signals (Fig. 4, the resistor chain of Rd coupled between VR63 and VR0); a pre-amp bank that receives the different input signal and the set of differential reference signals and outputs a set of differential output signals (Fig. 4, element 16, inputs VI and a reference voltage and outputs a differential signal from the amplifiers, A0–A63); a folding and interpolation circuit that receives the set of differential output signals and generates a set of differential folded signals (Fig. 3, elements 18 and 12); a course pre-amp that receives selected ones of the set of differential output signals and outputs a set of differential course output signals (Fig. 4, element 30 outputs coarse signals, element 28); a comparator bank that receives the set of differential folded signals and the set of differential course output signals and outputs a set of digitized fine signals and a set of digitized course signals (Fig. 3, elements 20 and 24); and a digital encoder that includes a fine decoder that converts the set of digitized fine signals into the least significant bits of the digital signal by setting the signals to a first logic level (Fig. 3, element 22). Van de Plassche outputs the most significant bits of the digital signal based on a second signal level from the coarse comparator circuit so there is inherently some sort of encoder circuit within the comparator (Fig. 3, element 24).

At the time of invention it would have been obvious to one of ordinary skill in the art to combine the teachings of Hara and van de Plassche to produce a graphics digitizer with an A/D converter using fine and coarse signals for producing a digital

output signal. The generic A/D converter of Hara could be replaced with the detailed fine and coarse signal A/D converter described by van de Plassche with the motivation of using an A/D converter that provides a good output with a smaller number of required components and no loss of speed or accuracy (van de Plassche, col. 2, lines 47-49). Thus, it would have been obvious to combine Hara and van de Plassche to create a graphics digitizer with a fine and coarse calculating A/D converter.

However, van de Plassche does not expressly disclose using an encoder circuit for setting the coarse digital signals.

Vorenkamp discloses an A/D converter with folding and interpolating that includes an input (Fig. 5, element Vi), reference voltage generator (Fig. 5, element IS), folding and interpolating circuits (Fig. 5, element IMS), fine and coarse generating circuits (Fig. 5, elements FLA and CLA respectively) and a digital encoder that takes in both fine and coarse signals for generating a final digital signal based on the fine and coarse input signals (Fig. 5, element ENC). The Examiner notes that the circuit of Vorenkamp is described as incorporating the A/D converter of van de Plassche for the generation of the fine and coarse signals (col. 7, lines 1-6).

At the time of invention it would have been obvious to one of ordinary skill in the art to combine the teachings of Hara, van de Plassche, and Vorenkamp to produce a graphics digitizer with an A/D converter using a digital encoder for encoding both the fine and coarse signals into a digital output. The combination would have been obvious based on the suggestion by Vorenkamp (col. 7, lines 1-6) of using the teachings of van de Plassche and Vorenkamp together to create a single A/D converter unit. Thus, it

would have been obvious to combine the teachings of Hara, van de Plassche, and Vorenkamp to produce a graphics digitizer using a specific A/D converter circuit.

Neither Hara, van de Plassche, nor Vorenkamp disclose the use of a sample and hold circuit for taking in the analog input signals before transmitting them to the rest of the analog-to-digital converter circuit. The Examiner takes Official Notice that the use of sample and hold circuits as an input stage of an analog-to-digital converter is well known in the art of A/D converters. It would have been obvious to one of ordinary skill in the art that a sample and hold circuit could have been used at the input of the A/D converters described by van de Plassche and Vorenkamp to holding the input signals before sending the signals to the pre-amp stage to being the conversion of the analog signals. Thus, it would have been obvious to combine the teachings of Hara, van de Plassche, and Vorenkamp to produce a graphics digitizer as described in claim 234.

Regarding claim 237, the logic levels output that represent the fine and coarse signals will be determined based on the input analog signal. Therefore, the first and second logic levels will be the same or different based on input data and how the data is converted in to fine and coarse signals. Thus, the combination of Hara, van de Plassche and Vorenkamp would also produce outputs from the fine and coarse comparators that would be either same or opposite polarities based on the coarse and fine signals that were generated.

5. Claims 238 and 240 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hara, van de Plassche, and Vorenkamp as applied to claim 234 above, and further in view of King et al. (USPN: 5382916), hereinafter King.

Regarding claim 238, the combination of Hara, van de Plassche, and Vorenkamp disclose all of the limitations except, "the digital decoder further includes an error correction circuit."

King discloses an A/D converter with fine and coarse calculation circuits that includes an error correction circuit (Fig. 3, element 318).

At the time of invention it would have been obvious to one of ordinary skill in the art to modify the teachings of Hara, van de Plassche, and Vorenkamp with the teachings of King. The motivation would be to provide an error correction circuit for correcting dynamic errors caused by the A/D converter during the fine and coarse conversion steps (King, col. 5, lines 50-56). Thus, it would have been obvious to combine the teachings of Hara, van de Plassche, Vorenkamp and King to produce the graphics digitizer described in claim 238.

Regarding claim 240, the A/D converter of King further includes a circuit indicator that indicates if the information is out of range based on an overflow or underflow condition (Fig. 3, element 324). This overflow and underflow correction circuit is a range correction circuit so that outputs that are too high or too low are corrected by the circuit.

Allowable Subject Matter

6. Claims 235 and 236 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claims 239 and 241 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven E. Holton whose telephone number is (571)272-7903. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steven E. Holton
Division 2629
August 17, 2008
/Bipin Shalwala/
Supervisory Patent Examiner, Art Unit 2629